EE/CprE/SE 491 WEEKLY REPORT 04
Oct 14 - Oct 20

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**

This week we continued work on the op-amp through design discussions and finding tradeoffs for certain designs. We also obtained the previous teams' git repos to see some of the cells they created and reasons for the choices they made. Also continued work on the basic 1T1R cell too.

- **Past week accomplishments**

  - Vinicius Malaman Soares: Discussed with Dr. Geiger, what to consider for op amp design. Research on different design methods we could follow for op amp design and their trade-offs.
  - Tyler Kloser: Decided the trade-offs for different ADC designs with respect to the sensitivity of the memresistor
  - Ali Mannan: Got into layout view and extraction the work of previous teams on the TIA and op-amp. Compiled the relevant process parameters for the Skywater 130nm PDK, this will be helpful in sizing transistors.
  - Austin Miller: Worked more on 1T1R module. Magic instantiates something for the reram cell sort of now. Also worked on website.

- **Pending issues**

  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: The reram thing that magic instantiates is likely wrong; it doesn't even seem to be using the reram material and doesn't behave like normal cells either
  - Vinicius Malaman Soares: N/A

Individual contributions

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Tyler Kloser	ADC designs and trade-offs	5	26
Ali Mannan	Extracted and worked with previous team designs for op-amp and TIA. Found and compiled Skywater 130nm process parameters.	5	35
Austin Miller	Reram cell troubleshooting, initial website setup	7	34
Vinicius Malaman Soares	Further research into op amp design and trade-offs	5	31

- **Comments and extended discussion** *(Optional)*

- **Plans for the upcoming week**

  Unless the advisors suggest otherwise, we intend on continuing work on the TIA for the project and the 1T1R design of a reRAM module. ADC designs will be considered for our application.

  - Ali Mannan: Complete LVS/DRC for op-amp and begin the precheck for TIA
  - Tyler Kloser: Work with team to start ADC design
  - Austin Miller: Get the reram cell either imported or created for 1T1R and other reram modules for magic
  - Vinicius Malaman Soares: Finish a Schematic for an op amp. Research for ADC design?

- **Summary of weekly advisor meeting**
  - Discussed some requirements in more detail, such as different versions of the same module for characterization (multiple modules, some with different sizes and such)
  - Discussed one of the biggest things we want to measure and/or compensate for is IR drop across the crossbar since this can change results of computations if we don't have linearity throughout.